

F1G. 1

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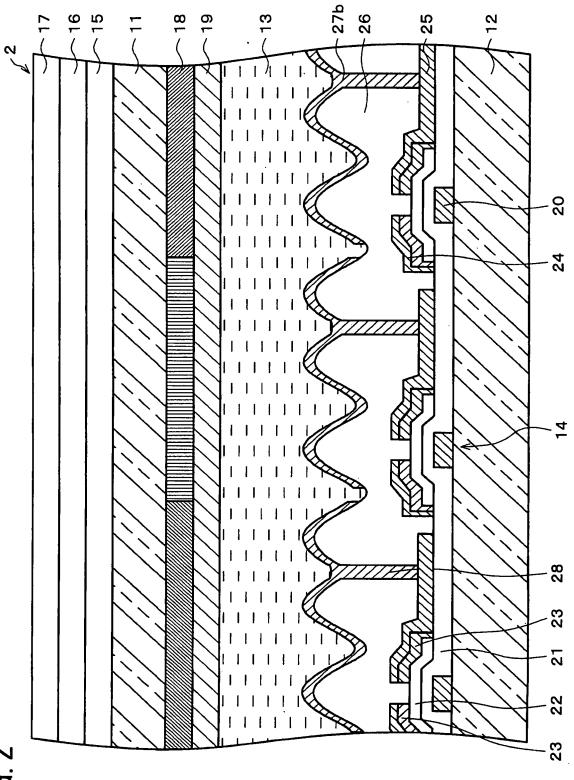
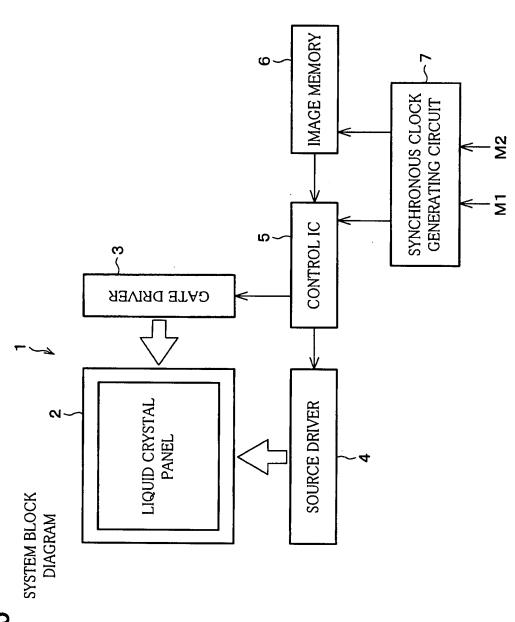


FIG.

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F16.

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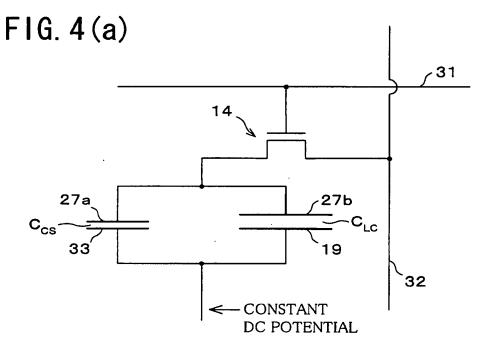
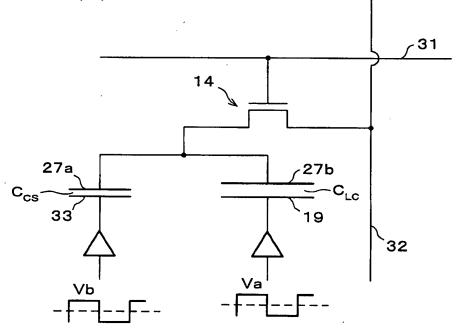


FIG. 4(b)



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FIG. 5(a)

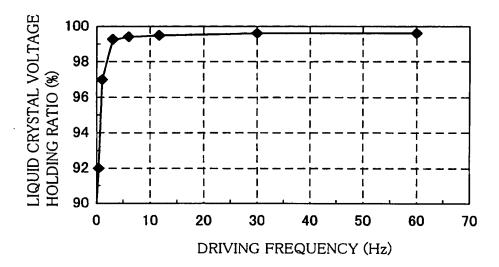
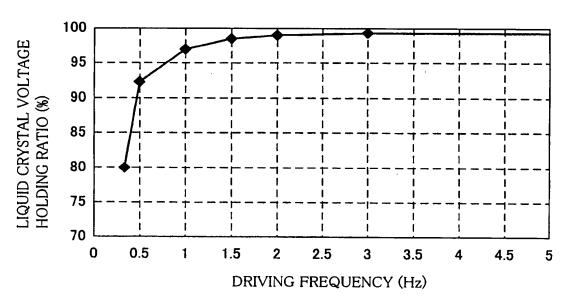
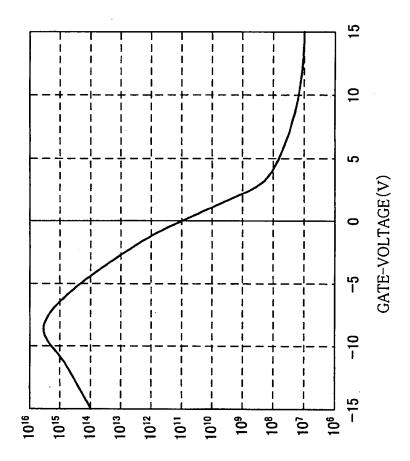


FIG. 5 (b)

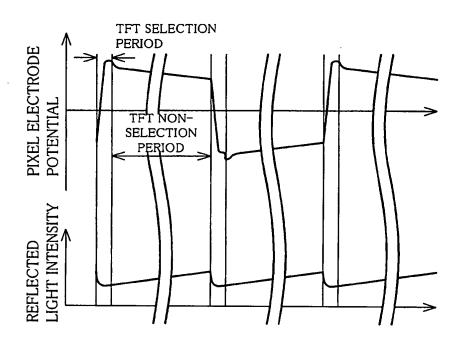




OFF-RESISTANCE (Q)

F1G. 6

FIG. 7



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FIG. 8(a)

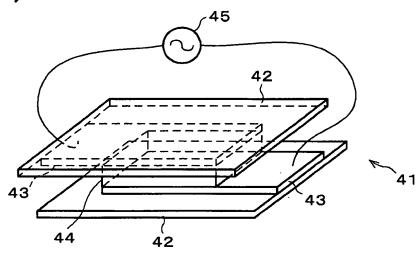
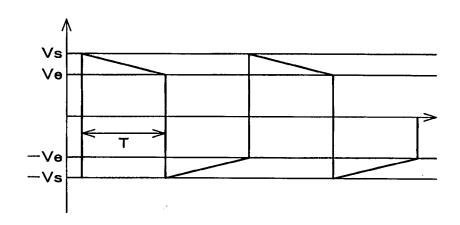
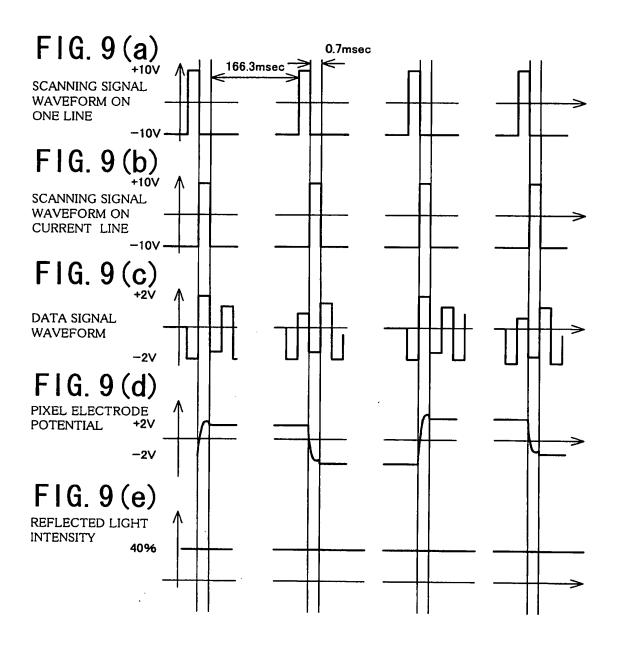
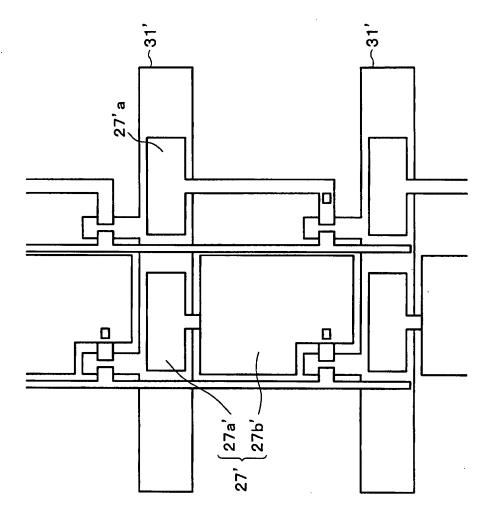


FIG. 8 (b)

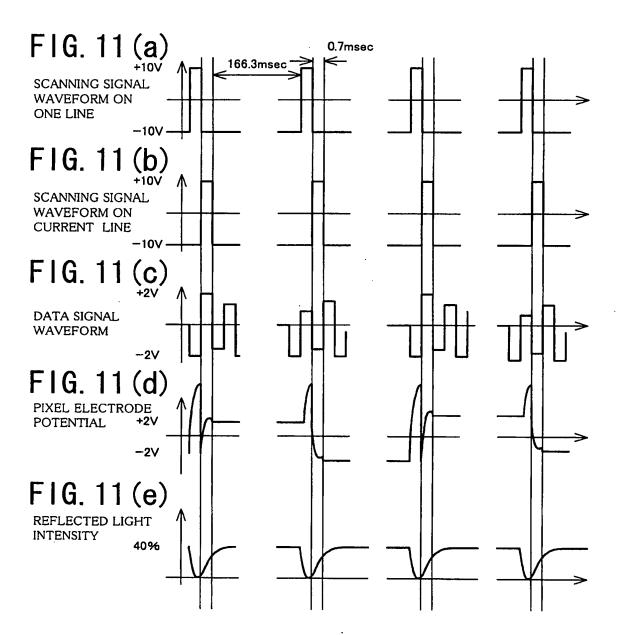


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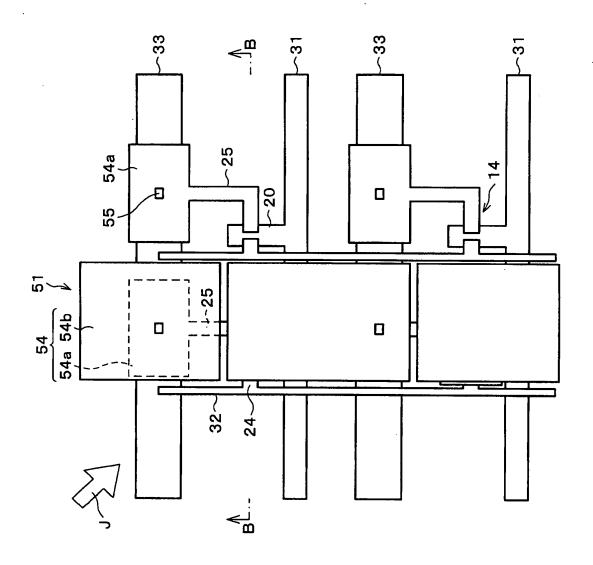




F1G. 10

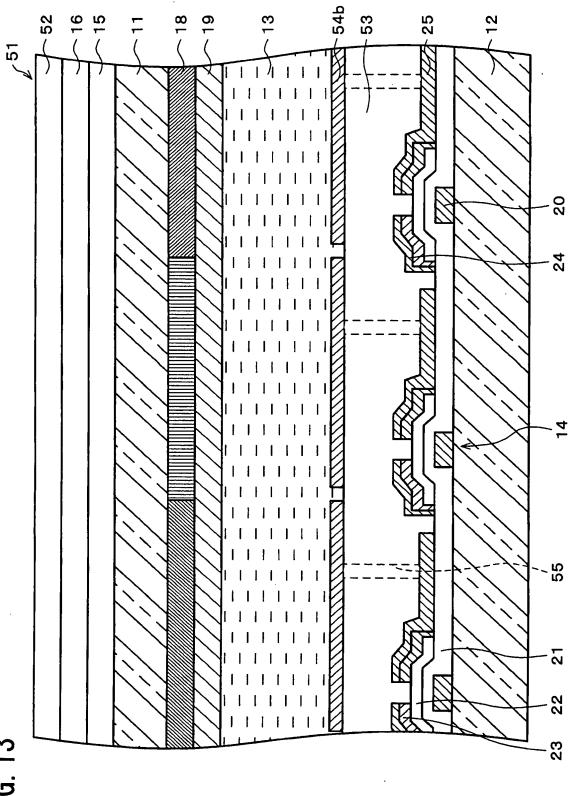


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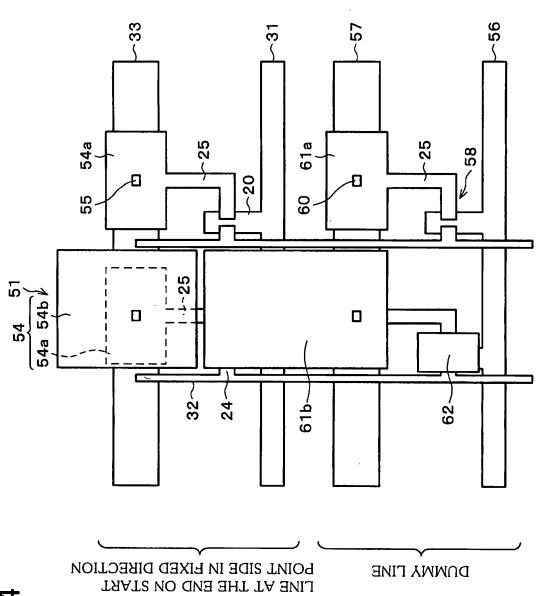


F1G. 12

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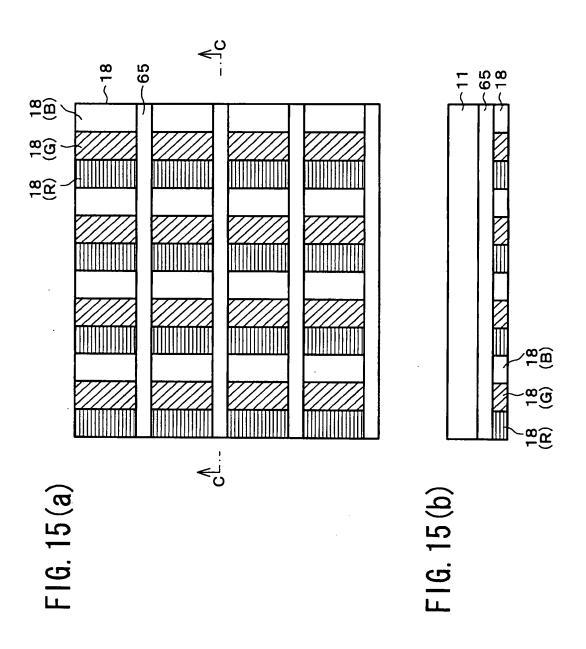


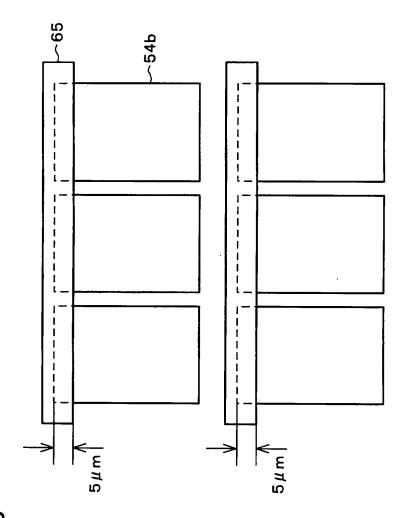
F1G. 13



F1G. 12

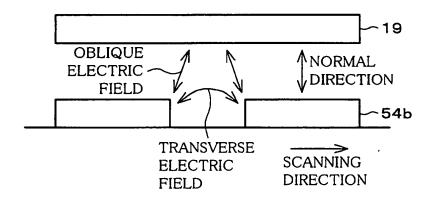
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F1G. 16

FIG. 17



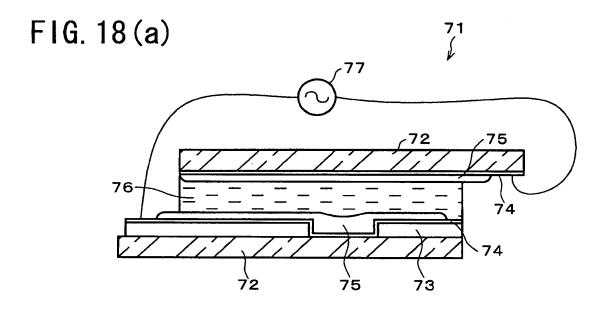
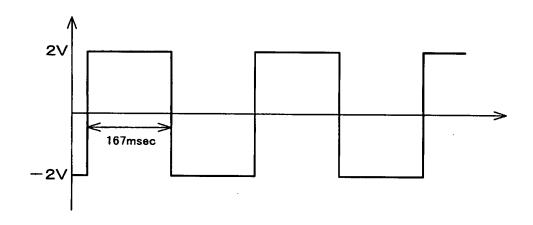
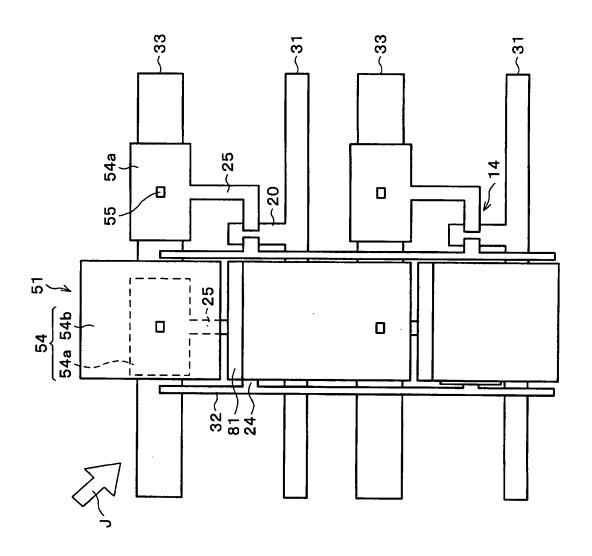


FIG. 18(b)

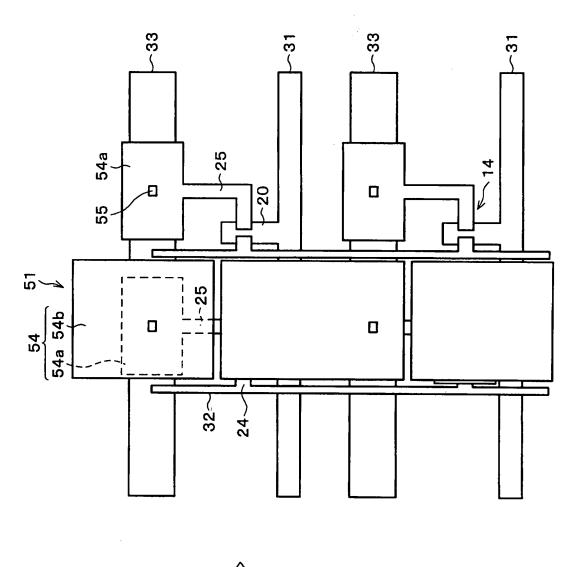


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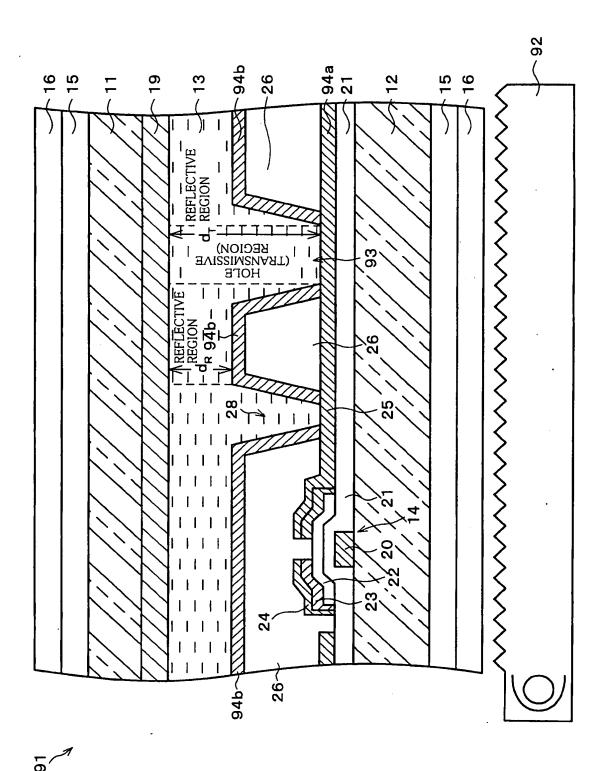
F1G. 19

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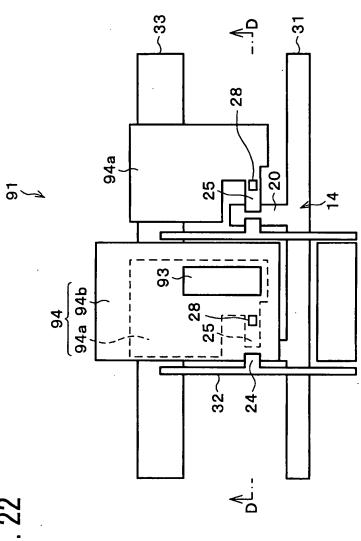


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F16. 21

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F1G. 22

FIG. 23

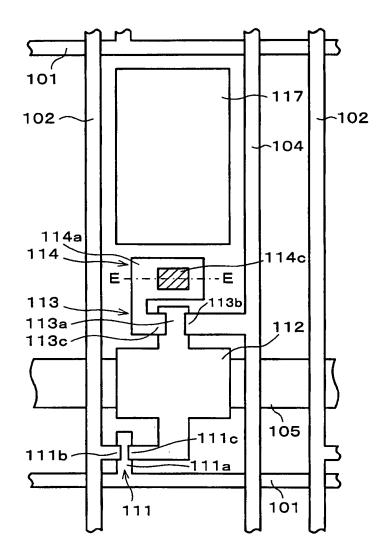
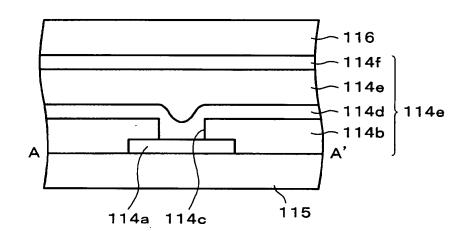


FIG. 24



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FIG. 25

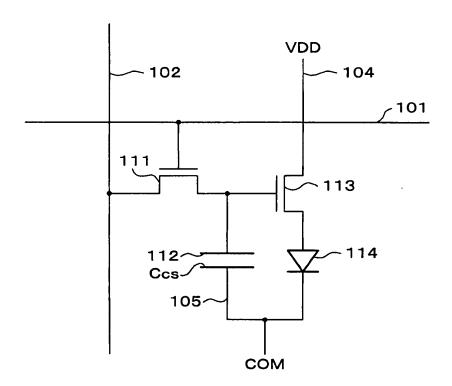
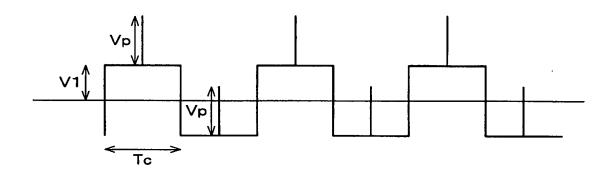


FIG. 26



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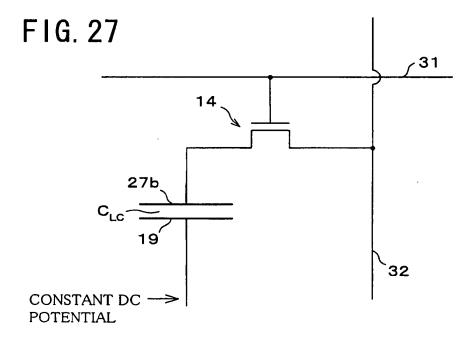
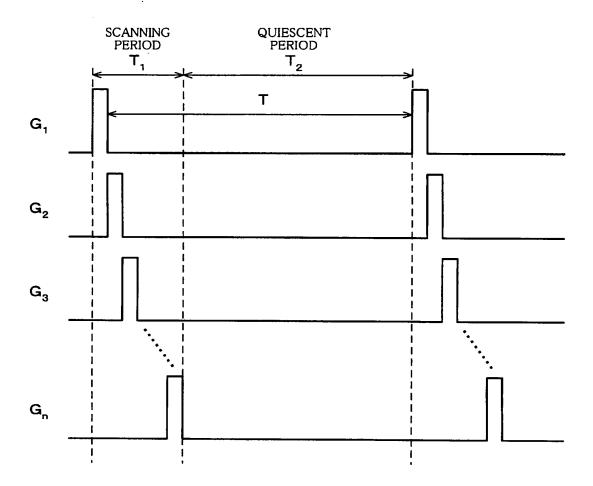
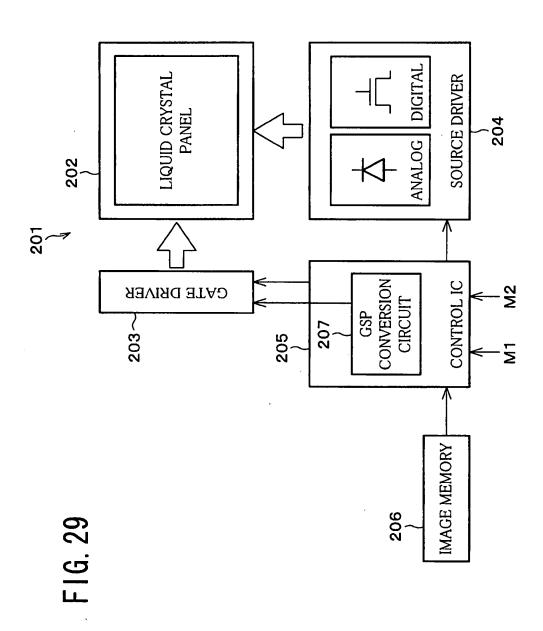


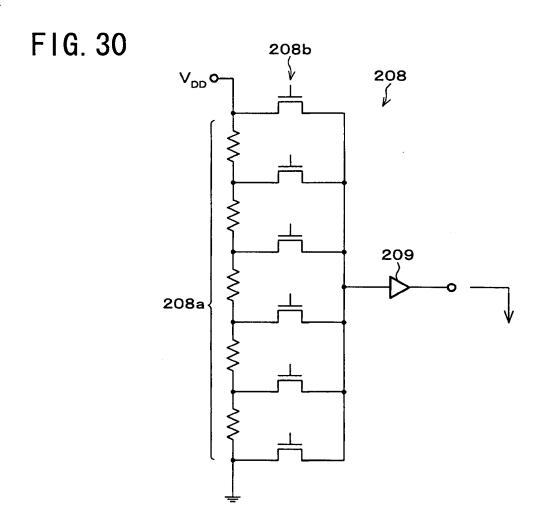
FIG. 28



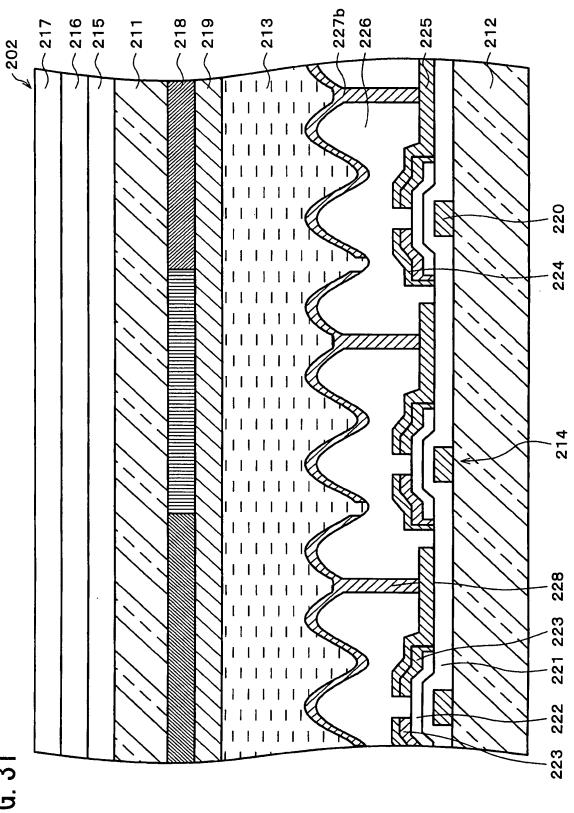
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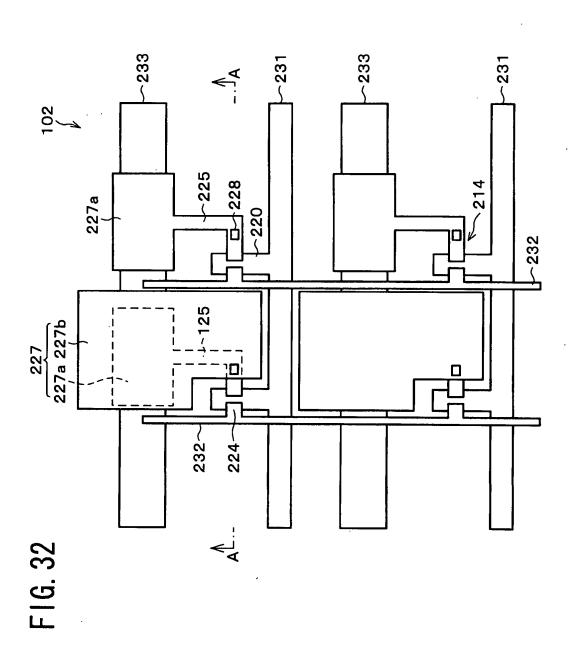


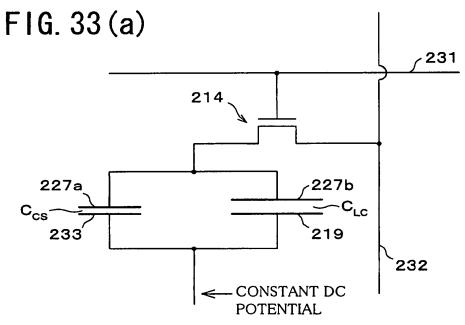
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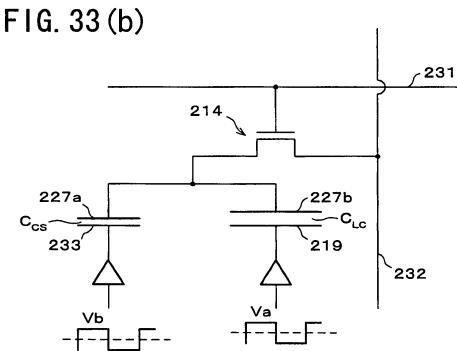


F1G. 31

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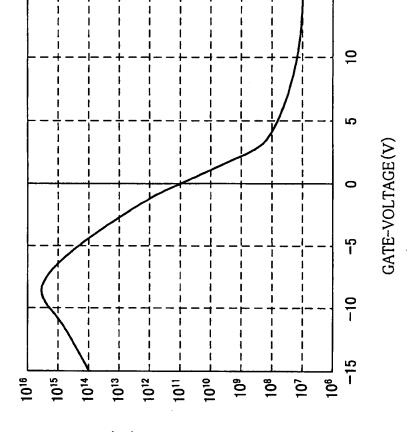


F1G. 34

100 PATIO 95 HOLDING PATIO (sec)

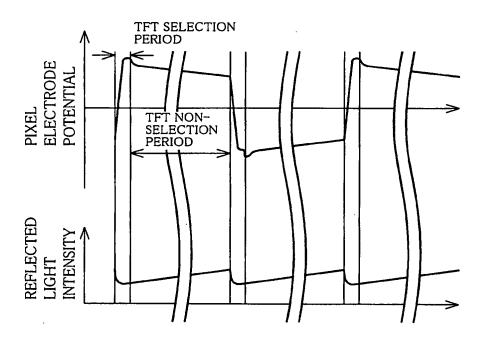
LIQUID CRYSTAL VOLTAGE

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OFF-RESISTANCE (Q)

FIG. 36



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FIG. 37(a)

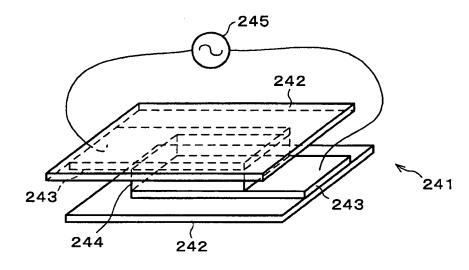
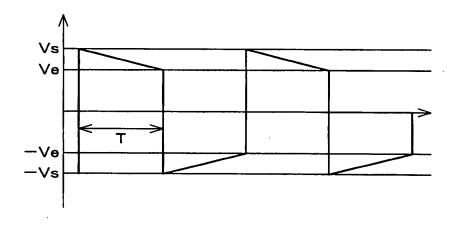
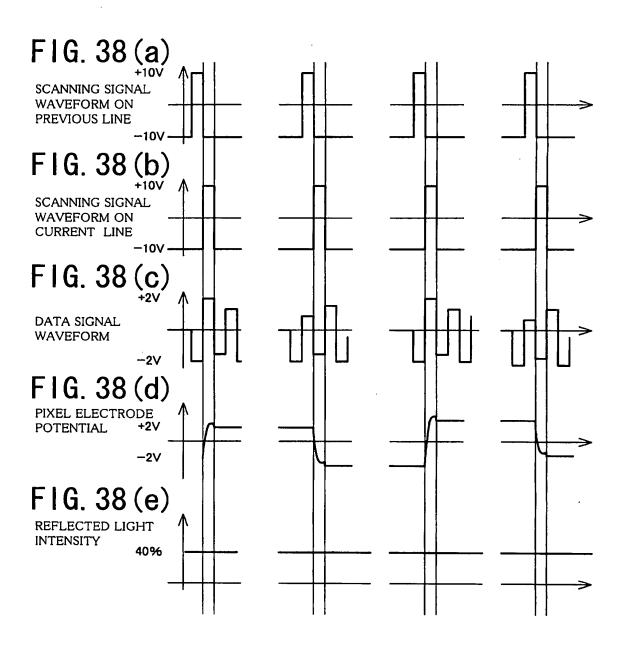
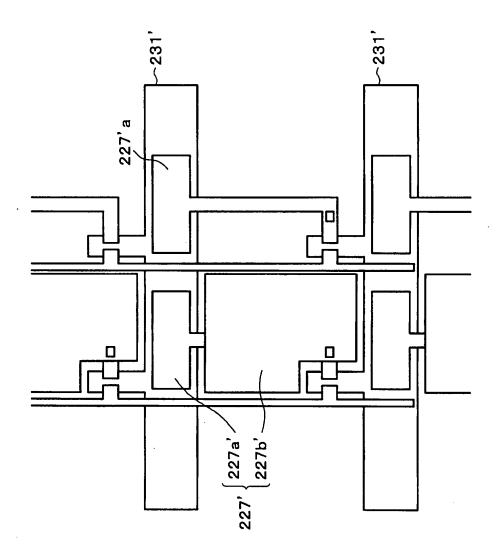


FIG. 37(b)

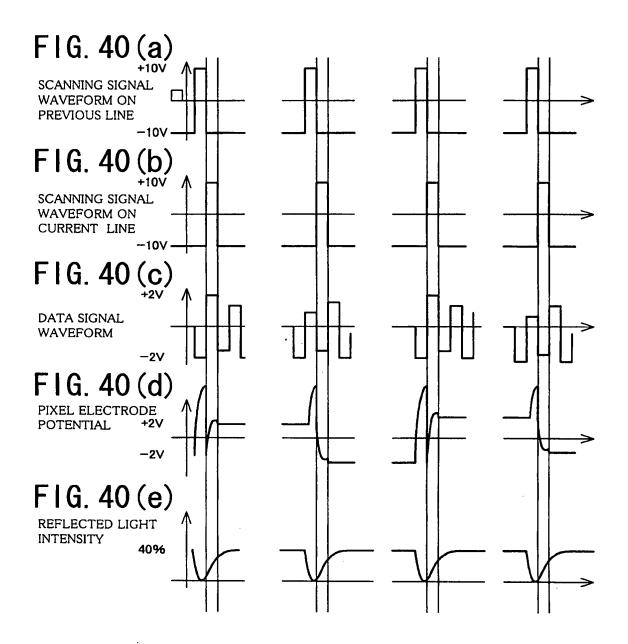




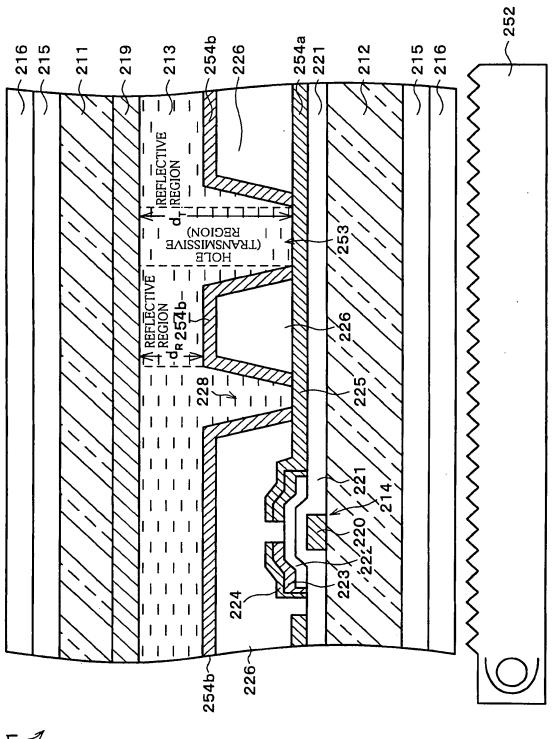
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F1G. 39



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F1G. 41

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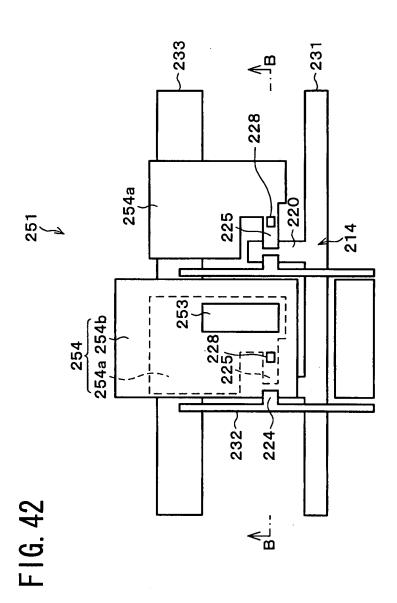


FIG. 43

		SOURCE DRIVER			
	<u> </u>	S(0)	S(1)	S(2)	S(3)
GATE DRIVER	G (0)	(0, 0)	(1, 0)	(2, 0)	(3, 0)
	G(1)	(0, 1)	(1, 1)	(2, 1)	(3, 1)
	G(2)	(0, 2)	(1, 2)	(2, 2)	(3, 2)
	G(3)	(0, 3)	(1, 3)	(2, 3)	(3, 3)

FIG. 44

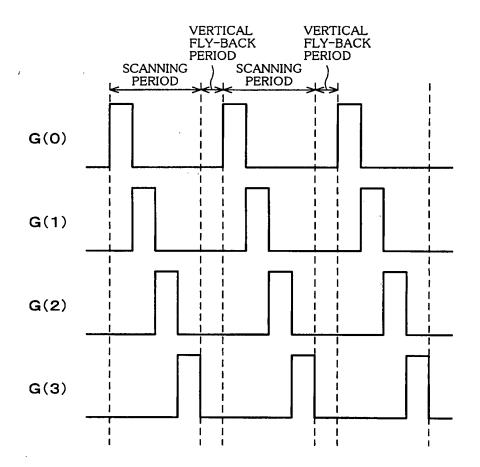
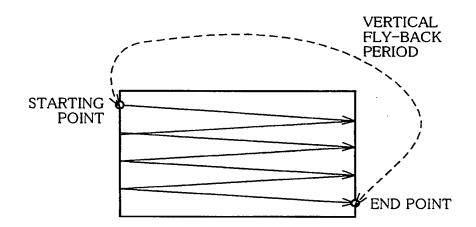
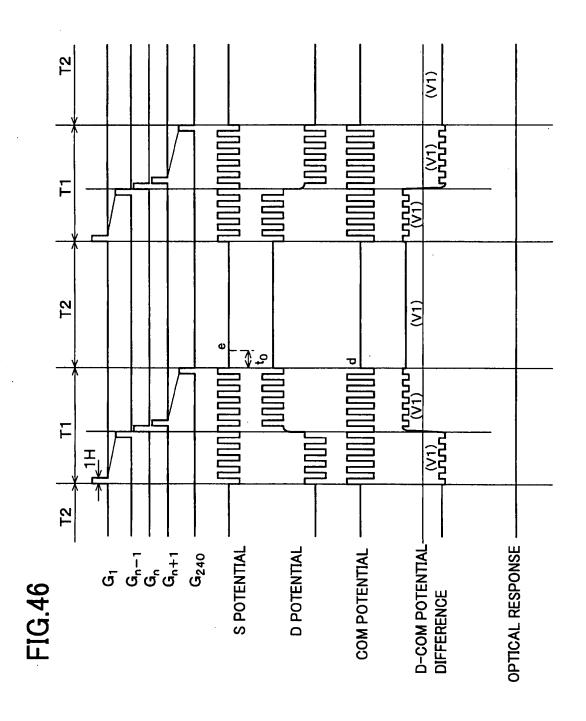
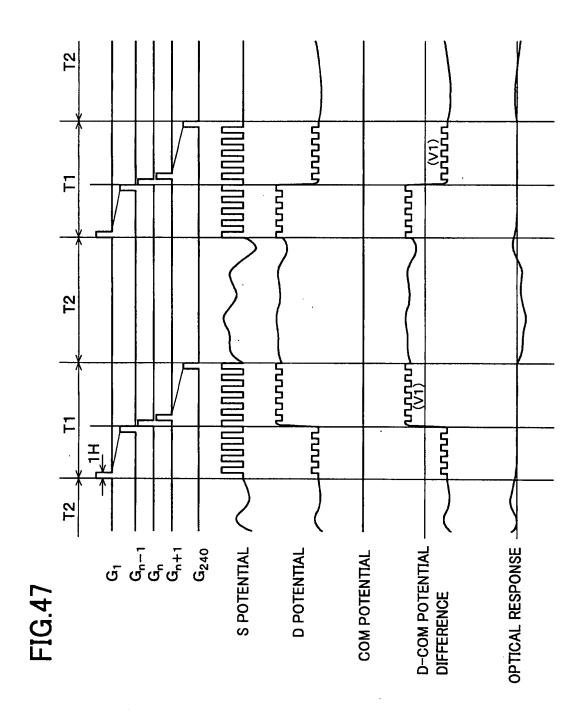
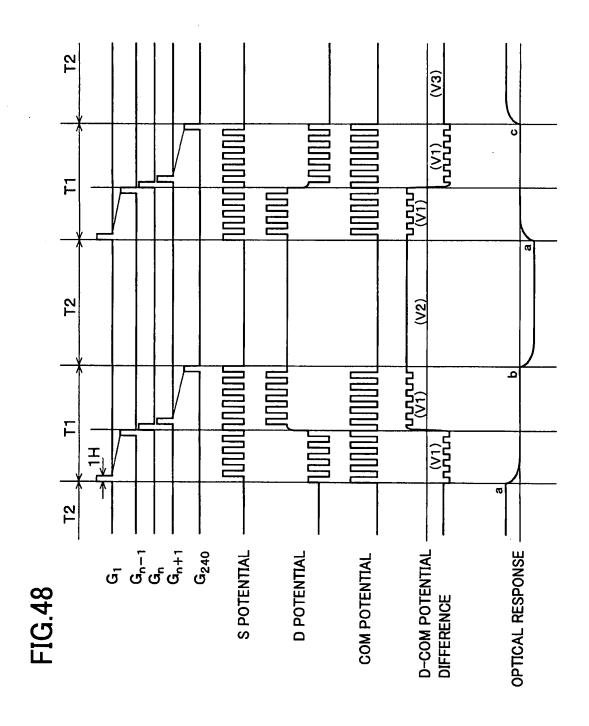


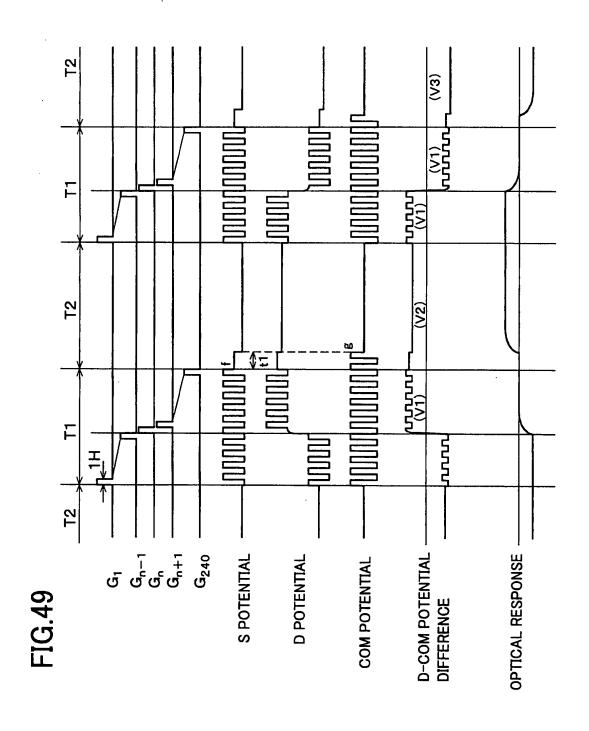
FIG. 45

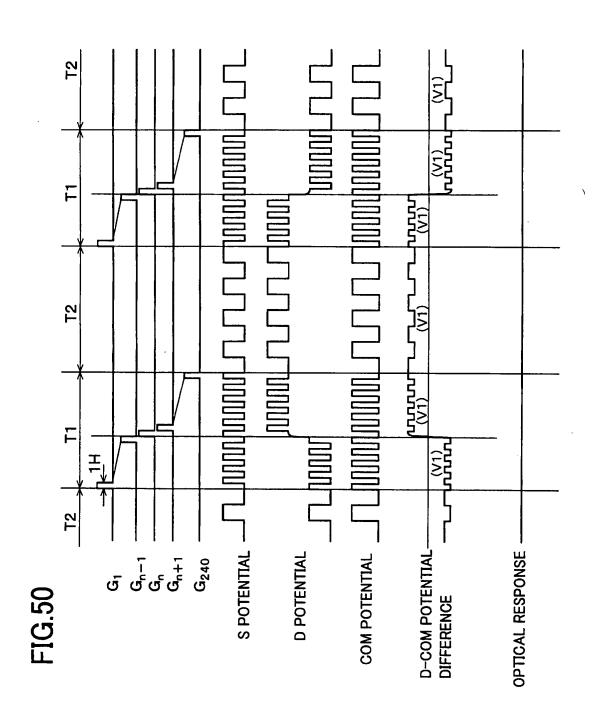


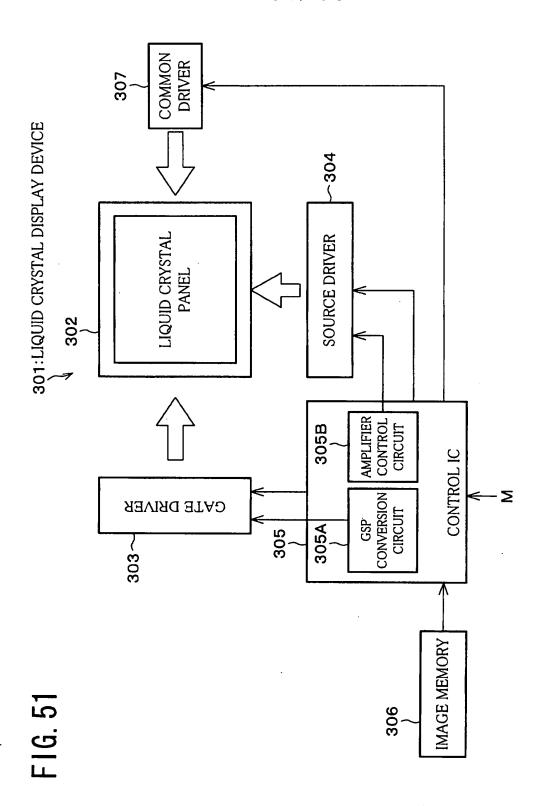


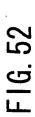


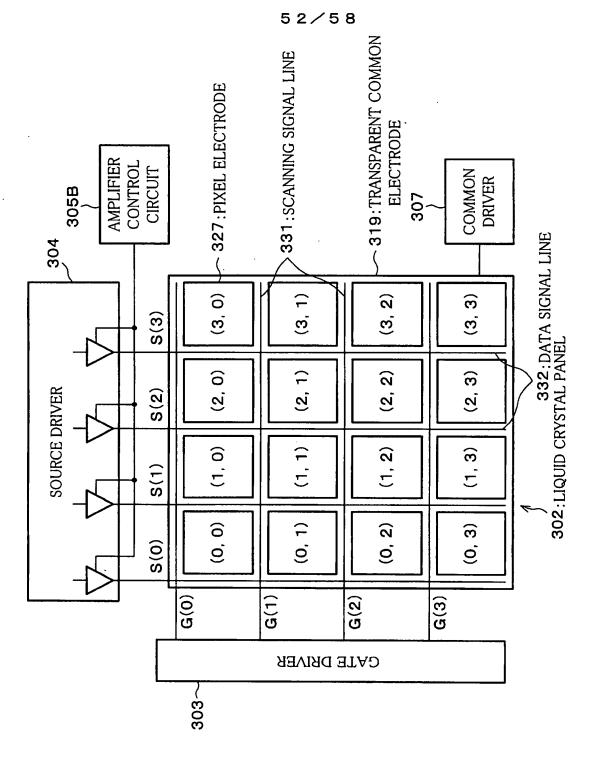




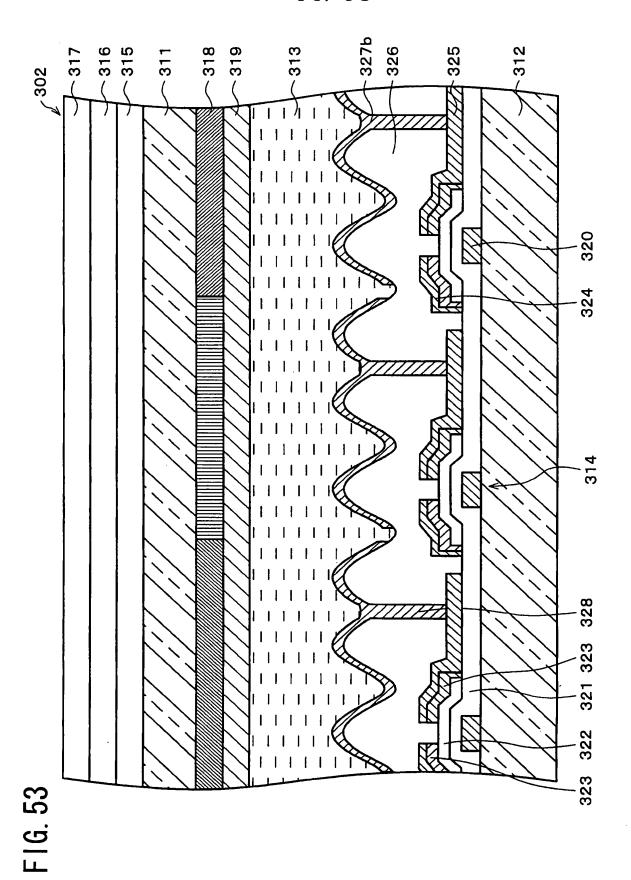








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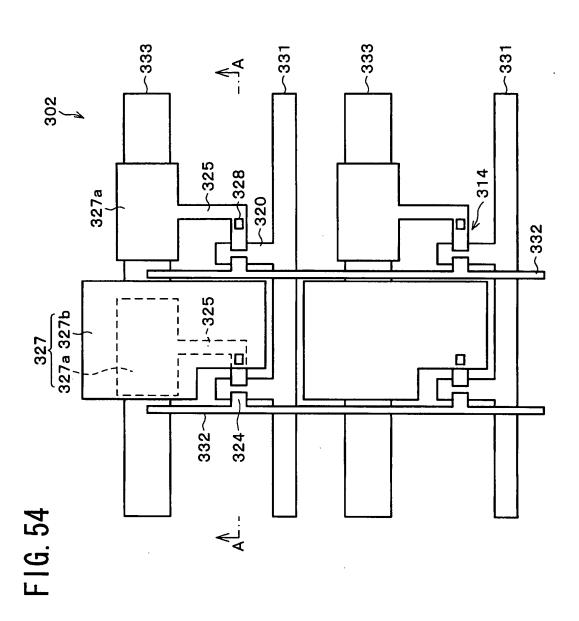
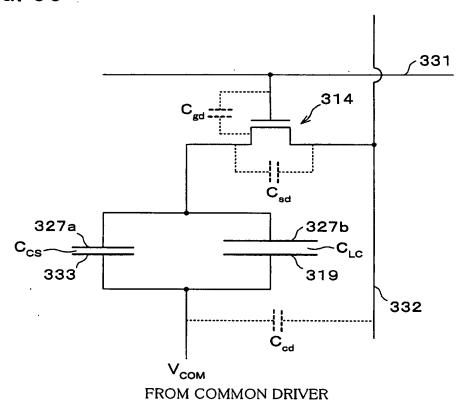
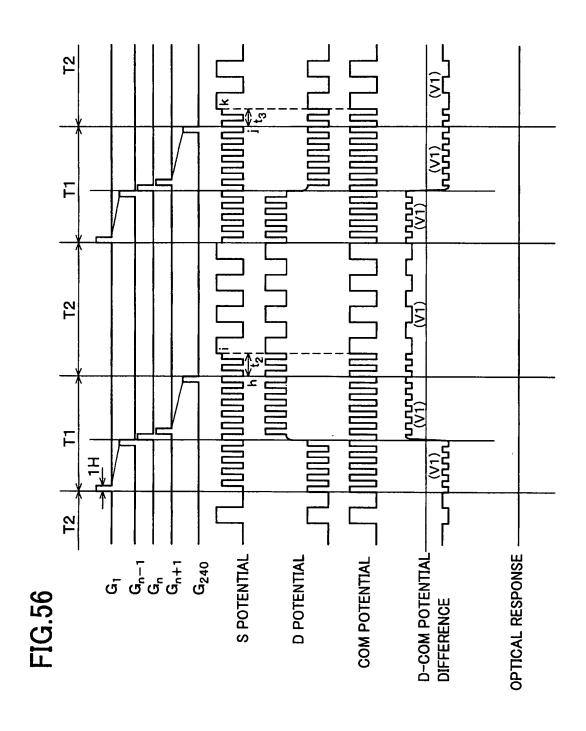
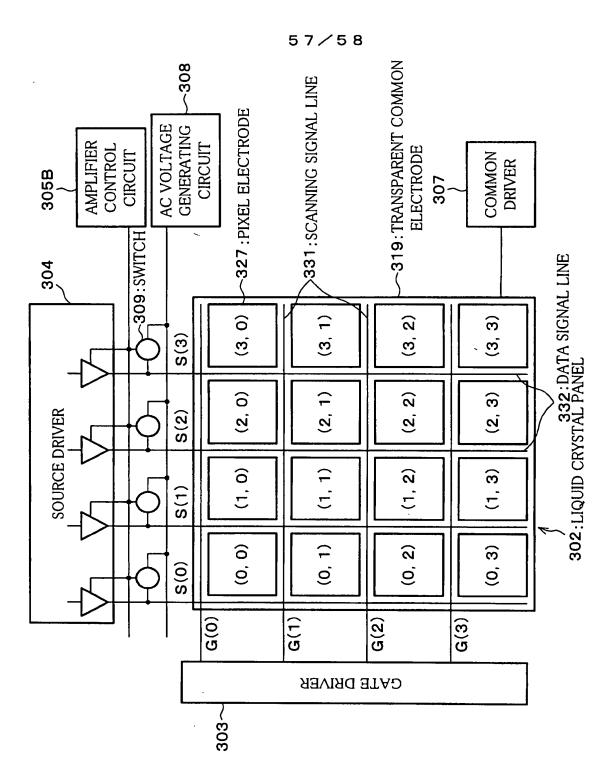


FIG. 55







F16.57

